AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An electronic component comprising at least one semiconductor chip having at least its electrodes formed exclusively on one surface thereof, and surfaces other than said one surface for each individual semiconductor chip are continuously covered with a protective material, and further wherein the protective material adjacent to side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent to the sides of the semiconductor chip, there being substantially none of the protective material formed on the one surface.

2. (Previously Presented) The electronic component according to claim 1 wherein said protective material comprises an organic insulating resin or an inorganic insulating material.

3. (Previously Presented) The electronic component according to claim 1, comprising a semiconductor chip diced from a wafer at a position of said protective material for mounting on a package substrate, wherein said electrode is formed on said one surface, which is a device surface, of said semiconductor chip, and both a side wall and a bottom surface of said semiconductor chip are covered with said protective material.

4. (Previously Presented) The electronic component according to claim 3 wherein a solder bump is formed on said electrode.

5. (Previously Presented) The electronic component according to claim 1 wherein a plurality of different types of semiconductor chips are integrated and bonded by said protective material.

6. (Currently Amended) A pseudo wafer comprising a plurality of semiconductor chips each having at least their electrodes formed solely on one surface thereof, wherein interspaces between between each individual one of said chips and bottom surfaces thereof are continuously covered with said protective material, and the chips are bonded with each other and further wherein the protective material adjacent the side surfaces of each semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chips, there being substantially none of the protective material formed on the one surface.

7. (Original) The pseudo wafer according to claim 6 wherein said protective material comprises either one of an organic insulating resin and an inorganic insulating material.

8. (Previously Presented) The pseudo wafer according to claim 6 wherein said plurality of semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality of semiconductor chips and thereafter mounted on a packaging substrate such that the protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip.

9. (Original) The pseudo wafer according to claim 8 wherein a solder bump is formed on said electrode.